



Scalable Techniques for Formal Verification

Sandip Ray

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This book is about formal verification, that is, the use of mathematical reasoning to ensure correct execution of computing systems. With the increasing use of computing systems in safety-critical and security-critical applications, it is becoming increasingly important for our well-being to ensure that those systems execute correctly. Over the last decade, formal verification has made significant headway in the analysis of industrial systems, particularly in the realm of verification of hardware. A key advantage of formal verification is that it provides a mathematical guarantee of their correctness (up to the accuracy of formal models and correctness of reasoning tools). In the process, the analysis can expose subtle design errors. Formal verification is particularly effective in finding corner-case bugs that are difficult to detect through traditional simulation and testing. Nevertheless, and in spite of its promise, the application of formal verification has so far been limited in an industrial design validation tool flow. The difficulties in its large-scale adoption include the following (1) deductive verification using theorem provers often involves excessive and prohibitive manual effort and (2) automated decision procedures (e. g. , model checking) can quickly hit the bounds of available time and memory. This book presents recent advances in formal verification techniques and discusses the applicability of the techniques in ensuring the reliability of large-scale systems. We deal with the verification of a range of computing systems, from sequential programs to concurrent protocols and pipelined machines.

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